

## MULTIPLE LEADFRAME LAMINATED IC PACKAGE

### FIELD OF THE INVENTION

**[0001]** This invention relates in general to integrated circuit packaging, and more particularly to a method for manufacture of an integrated circuit package.

### BACKGROUND OF THE INVENTION

**[0002]** High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by demands for increased thermal and electrical performance, decreased size and cost of manufacture.

**[0003]** Typically, array packaging such as ball grid array (BGA) packages provide for a high density package. Figure 1 shows a typical prior art package in which a copper leadframe 20 is etched to approximately half the leadframe thickness to form a pocket for the semiconductor die 22. The etch-down process results in an etch-down pocket with a radius 24 at each pocket corner (where the base 26 on which the semiconductor die 22 is mounted, meets each side 28). Each IC package includes a pocket that is large enough to accommodate the die 22 and the radius 24. Thus, the radius 24 limits the reduction in the size of the pocket.

**[0004]** Prior art IC packages such as that shown in Figure 1, are manufactured such that each of the contacts lie in a single plane. Thus, the solder ball contacts 30 on the leadframe lie in the same plane as the solder ball contacts 30 on the semiconductor die. The half etch depth of the leadframe 20 is important in order to ensure that all of the solder ball contacts 30 lie in a single plane. The half etch depth is difficult to accurately control and therefore manufacture of the IC package with solder ball contacts 30 in a single plane is difficult.

**[0005]** Accordingly, it is an object of an aspect of the present invention to provide a method for manufacturing an IC package that obviates or mitigates at least some of the disadvantages of the prior art.

### SUMMARY OF THE INVENTION

**[0006]** In one aspect of the present invention there is provided a method of fabricating an integrated circuit package. The method includes providing a first leadframe and a second leadframe, laminating the second leadframe to a portion of the first leadframe in order to

create a multi-layer laminated leadframe, and mounting a semiconductor die on another portion of the first leadframe.

**[0007]** In another aspect of the present invention there is provided an integrated circuit package. The integrated circuit package includes a first leadframe, a second leadframe laminated to a portion of the first leadframe in order to create a multi-layer laminated leadframe, and a semiconductor die mounted to another portion of the first leadframe.

**[0008]** In a particular aspect, the IC package of the present invention is manufactured without a large radius in the etch-down pocket of the leadframe strip. Advantageously, this permits reduced overall package size. Also, accurate control over manufacturing processes allows for planarity of the contacts.

**[0009]** In another aspect, the use of the solder contact balls is obviated by the use of solder plating on the leadframe strip. Also, die level solder bumps are replaced with copper plates. Advantageously, this package provides reduced electrical resistance to the electrical contacts, simpler and more cost effective construction.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** The present invention will be better understood with reference to the following drawings wherein like numerals refer to like parts throughout, and in which:

**[0011]** Figure 1 is a cross section of a typical prior art semiconductor die package;

**[0012]** Figures 2A to 2F show the processing steps for manufacturing an IC package in accordance with an embodiment of the present invention;

**[0013]** Figures 3A to 3F show the processing steps for manufacturing the IC package of Figure 1F in accordance with an alternative embodiment of the present invention;

**[0014]** Figures 4A to 4F show the processing steps for manufacturing an alternative IC package in accordance with another embodiment of the present invention;

**[0015]** Figures 5A to 5F show the processing steps for manufacturing the IC package of Figure 3F in accordance with an alternative embodiment of the present invention.

**[0016]** Figures 6A to 6G show the processing steps for manufacturing an IC package in accordance with another embodiment of the present invention;

**[0017]** Figures 7A to 7G show the processing steps for manufacturing the IC package of Figure 5F in accordance with an alternative embodiment of the present invention;

**[0018]** Figures 8A to 8G show the processing steps for manufacturing an IC package in accordance with yet another embodiment of the present invention; and

**[0019]** Figures 9A to 9G show the processing steps for manufacturing the IC package of Figure 6F in accordance with an alternative embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0020]** Reference is first made to Figures 2A to 2F to describe the processing steps for manufacturing an IC package in accordance with an embodiment of the present invention. Figure 2A shows a cross-sectional side view of a copper (Cu) panel substrate which forms the raw material of the leadframe strip indicated generally by the numeral 100. As discussed in greater detail in Applicants' U.S. Patent No. 6,229,200, the leadframe strip is divided into a plurality of sections, each of which incorporates a plurality of leadframe units in an array (e.g. 3 x 3 array, 5 x 5 array, etc.). Only one such unit is depicted in the cross-sectional view of Figure 2A.

**[0021]** As shown in Figure 2A, the copper strip is coated with a silver (Ag) plating on a bottom surface thereof and a solder plating on a top surface thereof. In one embodiment, the plating is a eutectic solder composition. This coating is added to enhance lamination and provide a surface for soldering.

**[0022]** Solder flux is added to a portion of the leadframe 100 (Figure 2B) and a second leadframe 102 with solder plating on both a top and a bottom surface thereof is laminated onto the first leadframe 100 using a proximity placement and thermal solder reflow technique to form a single pocket-type leadframe (Figure 2C). In an alternative embodiment the second leadframe is laminated onto the first leadframe using a hot roller thermo-compressive cladding process.

**[0023]** Next, the semiconductor die is mounted to the leadframe using known techniques. In the present embodiment, solder paste is dispensed on another portion of the first leadframe 100 in Figure 2D and the semiconductor die is attached to the first leadframe 100 by solder reflow technique (Figure 2E). The semiconductor die is coated with a suitable surface for soldering, such as titanium (Ti), tungsten (W), or gold (Au) for mounting via solder reflow. In an alternative embodiment, the die is attached using a silver-filled epoxy, as will be understood by those of skill in the art.

**[0024]** Next, solder ball contacts 106 are mounted on a vapor deposited layer referred to as "under bump metallurgy" or UBM on the semiconductor die 104, as will be understood by

those of skill in the art (Figure 2F).

**[0025]** Figures 3A to 3F show the processing steps for manufacturing the IC package of Figure 2F in accordance with an alternative embodiment of the present invention. The order of the process steps in the present embodiment is different from the order of the steps of the embodiment of Figures 2A to 2F. Figure 3A shows a cross-sectional side view of the copper (Cu) panel substrate which forms the raw material of the leadframe strip indicated generally by the numeral 100. Similar to the embodiment of Figures 2A, the copper strip is coated with a silver (Ag) plating on a bottom surface thereof and a solder plating on a top surface thereof.

**[0026]** Solder paste is dispensed on a portion of the leadframe 100 in Figure 3B and the semiconductor die 104 is attached to the leadframe 100 by solder reflow technique (Figure 3C). The semiconductor die 104 is coated with a suitable surface for soldering, such as titanium (Ti), tungsten (W), or gold (Au) for mounting via solder reflow. This is a solderable vapor deposit structure made in layers of three.

**[0027]** Next, solder flux is added to another portion of the first leadframe (Figure 3D) and a second leadframe 102 with solder plating on both a top and a bottom surface thereof is laminated onto the first leadframe 100 using a solder reflow technique to form a single pocket-type leadframe (Figure 3E).

**[0028]** The solder ball contacts 106 are then mounted on the semiconductor die 104 as shown in Figure 3F.

**[0029]** Figures 4A to 4F show the processing steps for manufacturing an alternative IC package in accordance with another embodiment of the present invention. The steps of Figures 4A to 4F are similar to the steps of Figures 2A to 2F except that the second leadframe 102 of the embodiment of Figures 4A to 4F is a different shape than the second leadframe 102 of the embodiment of Figures 2A to 2F. As shown in Figures 4B to 4F, the second leadframe 102 provides a pocket in the center of each unit in which the semiconductor die 104 is mounted, when laminated on the first leadframe 100.

**[0030]** Figures 5A to 5F show the processing steps for manufacturing the IC package of Figure 4F in accordance with an alternative embodiment of the present invention. The steps of Figures 5A to 5F are similar to the steps of Figures 3A to 3F except that the second leadframe 102 of the embodiment of Figures 3A to 3F is a different shape than the second leadframe 102 of the embodiment of Figures 3A to 3F. Again, the second leadframe 102 provides a pocket in the center of each unit in which the semiconductor die 104 is mounted when laminated on the first leadframe 100.

**[0031]** Figures 6A to 6G show the processing steps for manufacturing an IC package in accordance with another embodiment of the present invention. Figure 6A shows a cross-sectional side view of a copper (Cu) panel substrate which forms the raw material of the leadframe strip indicated generally by the numeral 100. The copper strip is coated with a silver (Ag) plating on a bottom surface thereof and a solder plating on a top surface thereof, as shown.

**[0032]** Next a solder flux is added to a portion of the first leadframe 100 (Figure 6B) and a second leadframe 102 with solder plating on both a top and a bottom surface thereof is laminated onto the first leadframe 100 using a solder reflow technique to form a single pocket-type leadframe (Figure 6C).

**[0033]** Solder paste is then dispensed on a portion of the first leadframe 100 (Figure 6D) and the semiconductor die is attached to the first leadframe 100 by solder reflow technique (Figure 6E). The semiconductor die is coated with a suitable surface for soldering, such as titanium (Ti), tungsten (W), or gold (Au) for mounting via solder reflow.

**[0034]** Next, portions of the semiconductor die are coated with solder flux (Figure 6F) and a third leadframe 108 with solder plating on both top and a bottom surfaces thereof is laminated to coated contact pads or I/O pads on the surface of the semiconductor die (Figure 6G) via solder reflow technique. In an alternative embodiment the third leadframe 108 is laminated to the coated contact pads of the semiconductor die by epoxy. The contact pads are coated with, for example, Ti, W, or Au, for compatibility with the solder or with epoxy.

**[0035]** Figures 7A to 7G show the processing steps for manufacturing the IC package of Figure 6G in accordance with an alternative embodiment of the present invention. The order of the process steps in the present embodiment is different from the order of the steps of the embodiment of Figures 6A to 6G. Figure 7A shows a cross-sectional side view of the copper (Cu) panel substrate, which forms the raw material of the leadframe strip, indicated generally by the numeral 100. Similar to the embodiment of Figures 6A, the copper strip is coated with a silver (Ag) plating on a bottom surface thereof and a solder plating on a top surface thereof.

**[0036]** Solder paste is dispensed on a portion of the leadframe 100 (Figure 7B) and the semiconductor die 104 is attached to the leadframe 100 by solder reflow technique (Figure 7C). The semiconductor die 104 is coated with a suitable surface for soldering, such as titanium (Ti), tungsten (W), or gold (Au) for mounting via solder reflow.

**[0037]** Next, solder flux is dispensed on another portion of the leadframe 100 (Figure

7D) and a second leadframe 102 having solder plating on both a top and a bottom surface thereof is laminated onto the first leadframe 100 using a solder reflow technique to form a single pocket-type leadframe (Figure 7E).

**[0038]** Solder flux is then dispensed onto portions of the semiconductor die 104 (Figure 7F) and a third leadframe 108 with solder plating on both top and bottom surfaces is laminated on the surface of the semiconductor die.

**[0039]** Figures 8A to 8G show the processing steps for manufacturing an alternative IC package in accordance with another embodiment of the present invention. The steps of Figures 8A to 8G are similar to the steps of Figures 6A to 6G except that the second leadframe 102 of the embodiment of Figures 8A to 8G is a different shape than the second leadframe 102 of the embodiment of Figures 6A to 6G. As shown in Figures 8B to 8G, the second leadframe 102 provides a pocket in the center of each unit in which the semiconductor die 104 is mounted, when laminated on the first leadframe 100.

**[0040]** Figures 9A to 9G show the processing steps for manufacturing the IC package of Figure 8G in accordance with an alternative embodiment of the present invention. The steps of Figures 9A to 9G are similar to the steps of Figures 7A to 7G except that the second leadframe 102 of the embodiment of Figures 9A to 9G is a different shape than the second leadframe 102 of the embodiment of Figures 7A to 7G. Again, the second leadframe 102 provides a pocket in the center of each unit in which the semiconductor die 104 is mounted when laminated on the first leadframe 100.

**[0041]** Alternative embodiments and variations are possible. For example, in an alternative embodiment, the semiconductor die is attached to the leadframe by reflow of the solder plated on the copper of the first leadframe 100 rather than by the addition of solder paste to the leadframe and subsequent reflow. In yet another alternative embodiment, the semiconductor die is mounted on the leadframe via silver epoxy. Other embodiments and variations will occur to those of skill in the art. All such embodiments and variations are believed to be within the scope and sphere of the present invention as defined by the claims appended hereto.